1. A capacitor, comprising:

a high-k dielectric material disposed between a first terminal and a second terminal;

the first terminal comprising a first material which substantially prevents diffusion of copper therethrough, and a second material, superjacent the first material, which substantially prevents diffusion of oxygen and oxygen-containing compounds therethrough; and

the second terminal comprising a third material which substantially prevents diffusion of oxygen and oxygen-containing compounds therethrough, and a fourth material, superjacent the first material, which substantially prevents diffusion of copper therethrough.

2. The capacitor of Claim 1, wherein the first material is selected from the group consisting of TiN and TaN.

3. The capacitor of Claim 1, wherein the second material is selected from the group consisting of Pt, Ir, and Ru.

4. The capacitor of Claim 1, wherein the third material is selected from the group consisting of Pt, Ir, and Ru.

5. The capacitor of Claim 1, wherein the fourth material is selected from the group consisting of TiN and TaN.

6. The capacitor of Claim 1, wherein the first and second material are the same.

7. The capacitor of Claim 1, wherein the second terminal further comprises a fifth material superjacent the fourth material, and the fourth and fifth materials have different etch rates in a fluorine-containing plasma.

8. The capacitor of Claim 1, wherein the second terminal further comprises a fifth material superjacent the fourth material, and the fourth and fifth materials have different etch rates in a chlorine-containing plasma.

9. The capacitor of Claim 1, wherein the first terminal is non-planar, and the second terminal is conformal to the first terminal.

10. The capacitor of Claim 9, wherein the first terminal is disposed upon a non-planar conductive layer.

11. An integrated circuit, comprising:

a plurality of interconnected components disposed in a substrate;

a first interconnect line disposed on a first interconnect level of the substrate, and a second interconnect line disposed on a second interconnect level of the substrate;

a capacitor having a first terminal in electrical contact with the first interconnect line, and further having a second terminal in electrical contact with the second interconnect line;

the capacitor comprising a high-k dielectric material disposed between a first terminal and a second terminal;

the first terminal comprising a first material which substantially prevents diffusion of copper therethrough, and a second material, superjacent the first material, which substantially prevents diffusion of oxygen and oxygen-containing compounds therethrough; and

the second terminal comprising a third material which substantially prevents diffusion of oxygen and oxygen-containing compounds therethrough, and a fourth material, superjacent the first material, which substantially prevents diffusion of copper therethrough.

12. The integrated circuit of Claim 11, wherein the first and second interconnect lines comprise copper.

13. The integrated circuit of Claim 12, wherein the second material comprises a material selected from the group consisting of platinum, iridium, and ruthenium.

14. The integrated circuit of Claim 12, wherein the third material comprises a material selected from the group consisting of platinum, iridium, and ruthenium.

15. The integrated circuit of Claim 12, wherein the second terminal further comprises a fifth material superjacent the fourth material.

16. The integrated circuit of Claim 15, wherein the fifth material is selected from the group consisting of aluminum and tungsten.

17. A method of forming a capacitor, comprising:

forming an in-laid conductor structure on a substrate; the in-laid conductor structure including an intra-layer dielectric;

forming a first layer over the conductor;

forming a second layer over the first layer;

forming a third layer over the second layer;

forming a patterned masking layer over the third layer such that a portion of the third layer is exposed, and patterning the third, second and first layers in alignment with the masking layer, so as to form a vertical stack superjacent the conductor; and

forming a second conductor over the vertical stack.

18. The method of Claim 17, wherein the first layer comprises tantalum, the second layer comprises tantalum pentoxide, and the third layer comprises tantalum.

19. The method of Claim 18, wherein the in-laid conductor and the second conductor comprise copper.

20. The method of Claim 17, wherein forming the first layer comprises depositing tantalum.

21. The method of Claim 17, wherein forming the second layer comprises depositing tantalum pentoxide.

22. The method of Claim 21, wherein forming the third layer comprises depositing tantalum.

23. The method of Claim 17, further comprising forming an electrically insulating layer over the third layer and patterning the insulating layer so as to expose portions of the third layer prior to forming the second conductor.

24. The method of Claim 23, wherein forming a second conductor over the vertical stack includes making electrical contact between the second conductor and the third layer.

25. A method of forming a capacitor, comprising:

forming a plurality of in-laid conductors on a substrate;

selectively depositing a first conductive material over the plurality of in-laid conductors;

blanket depositing a layer of high-k dielectric material over the substrate;

blanket depositing a second conductive material over the high-k dielectric material; and

patterning the second conductive material and the high-k dielectric material.

26. The method of Claim 25, wherein patterning the second conductive material and the high-k dielectric material comprises etching the second conductive material and the high-k dielectric material such that they are removed from a portion of the underlying plurality of in-laid conductors.

27. The method of Claim 26, wherein the in-laid conductors comprise copper.

28. The method of Claim 27, wherein the first and second conductors comprise tantalum and the high-k dielectric material comprises tantalum pentoxide.

29. The method of Claim 27, wherein the high-k dielectric material comprises barium strontium titinate.

30. A method of forming a capacitor, comprising:

forming a plurality of in-laid conductors on a substrate;

blanket depositing a first conductive material over the plurality of in-laid conductors;

blanket depositing a layer of high-k dielectric material over the substrate;

blanket depositing a second conductive material over the high-k dielectric material;

blanket depositing a third conductive material over the second conductive material;

forming a patterned layer of photoresist over the third conductive material so as to expose portions of the third conductive material;

etching the exposed portions of the third conductive material and removing the photoresist; and

etching the second conductive material, the high-k dielectric layer, and the first conductive material, using the third conductive material as a hardmask.

31. The method of Claim 30, wherein the third conductive material comprises aluminum, and etching the second conductive material, the high-k dielectric layer, and the first conductive material comprises etching with a fluorine based plasma.

32. The method of Claim 31, wherein the high-k dielectric comprises an oxide of tantalum.

33. The method of Claim 30, wherein the third conductive material comprises tungsten, and etching the second conductive material, the high-k dielectric layer, and the first conductive material comprises etching with a fluorine based plasma.

34. The method of Claim 33, wherein the high-k dielectric comprises barium strontium titinate.

35. The method of Claim 32, wherein the first conductive material is a barrier to copper diffusion.

36. The method of Claim 34, wherein the first conductive material is a barrier to copper diffusion.